Notice of Allowability	Application No.	Applicant(s)	
	10/063,788	SAKAGUCHI ET AL.	
	Examiner	Art Unit	
	VIJAY SHANKAR	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed on 2-21-2006*.

2. ☒ The allowed claim(s) is/are *1-6, 9-20, Renumbered as 1-18*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

VIJAY SHANKAR
Primary Examiner
Art Unit: 2629

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Allowable Subject Matter

2. Claims 1-6 and 9-20 are allowed.

3. The following is an examiner's statement of reasons for allowance: The prior arts Sakaguchi et al (6,806,861), Buhr et al (5,528,339) fails to recite or disclose the uniquely distinct features, a liquid crystal display driver **wherein the driver comprises a pulse generation circuit for generating a plurality of reference pulses in which pulse generation densities are weighted; and the pulse select/ synthesis circuit outputs a logical sum between a carry output from an adder circuit, which has as its inputs high order W bits of the digital input data of n bits and low order W bits of a binary counter, and a logical product between outputs X(m-1) through X(0) of the pulse generation circuit where m=n-W and the digital input data D(m-1) through D(O) as claimed in Claims 1,4,5.**

The prior arts Sakaguchi et al (6,806,861), Buhr et al (5,528,339) fails to recite or disclose the uniquely distinct features, a reference pulse generation circuit for generating reference pulses corresponding to n-bit digital input data, comprising: **an n-**

bit binary counter for counting up in synchronization with an input clock; an n-1 bit latch for generating signals by delaying high order n-1 bits output B (n-1) through B(1) from the binary counter by one input clock period; and n-1 logical circuits for performing logical operations with receiving as inputs the high order n-1 bits output B(n-1) through B(1) from the binary counter and the delayed signals corresponding to the high order n-1 bits output B(n-1) through B(1) from the n-1 bit latch and obtaining outputs X(0) through X(n-2) with lower reference pulse densities, whereas output X(n-1) is obtained bypassing the logical circuit, wherein the pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding lo the digital input data, and wherein the n-1 logical circuits are n-1 AND circuits, and the n-1 logical circuits are n-2 AND circuits outputting X(0) through X(n-3) and a NOR circuit outputting X(n-2) ad claimed in Claims 10-12.

The prior arts Sakaguchi et al (6,806,861), Buhr et al (5,528,339) fails to recite or disclose the uniquely distinct features, a liquid crystal display driver comprising **an integration circuit for integrating the pulse string generated by the pulse select/synthesis circuit to output a voltage for gamma correction, wherein the pulse select/ synthesis circuit outputs a logical sum between a carry output from an adder circuit, which has as its inputs high order W bits of the digital input data of n bits and low order W bits of a binary counter, and a logical product between outputs X(m-1) through X(0) of the pulse generation circuit**

where m=n-W and the digital input data D(m-1) through D(O), and wherein if the digital input data is n bits, then the pulse generation circuit outputs the reference pulses using an n-bit binary counter, an n-1 bit latch, and n-1 2-input gates as claimed in Claims 6,13,15,17, 19.

The prior arts Sakaguchi et al (6,806,861), Buhr et al (5,528,339) fails to recite or disclose the uniquely distinct features, a reference pulse generation circuit for generating reference pulses corresponding to n-bit digital input data, comprising: **an n-bit binary counter for counting up in synchronization with an input clock; an n-1 bit latch for generating signals by delaying high order n-1 bits output B (n-1) through B(1) from the binary counter by one input clock period; and n-1 logical circuits for performing logical operations with receiving as inputs the high order n-1 bits output B(n-1) through B(1) from the binary counter and the delayed signals corresponding to the high order n-1 bits output B(n-1) through B(1) from the n-1 bit latch and obtaining outputs X(0) through X(n-2) with lower reference pulse densities, whereas output X(n-1) is obtained bypassing the logical circuit, wherein the pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding lo the digital input data, and wherein the n-1 logical circuits are n-1 AND circuits, and the n-1 logical circuits are n-2 AND circuits outputting X(0) through X(n-3) and a NOR circuit outputting X(n-2) ad claimed in Claim 20.**

The closest prior art, Sakaguchi et al (6,806,861), Buhr et al (5,528,339), either singularly or in combination, fail to anticipate or render the above bold and underlined limitations obvious.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIJAY SHANKAR whose telephone number is (571) 272-7682. The examiner can normally be reached on M-F 7:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIJAY SHANKAR
Primary Examiner
Art Unit 2673

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